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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/678,685	DOUMA ET AL.	
	Examiner	Art Unit	
	Linda Wong	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Regarding the 35 USC 112 rejection, due to the amendments to the claims rejected under 35 USC 112, the rejection is withdrawn.

2. Applicant's arguments filed 5/11/2007 have been fully considered but they are not persuasive.

   a. The applicant contends

   > "Claim 14 recites, among other things, "receiving an asserted synchronization signal from a phase locked loop ... [and] determining whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency ...." In contrast, the Examiner has not established that Wang teaches the aforementioned limitations.
   >
   > The Examiner asserted that Wang discloses the aforementioned limitations in the abstract and at paragraph [0053]. See Office Action, p. 2 (citing Wang at abstract, lines 5-6, 9-11, 12-15). Applicants respectfully disagree. The abstract describes a "frequency phase-locked loop detector(17) for supplying an output signal indicating whether an intermediate frequency demodulator is in an unlocked mode ... or in a locked mode" and "a video detector (18) for detecting a video property in the incoming signal." As a preliminary matter, it is unclear what portion of the cited passages corresponds to the claimed "asserted synchronization signal" and clarification is respectfully requested. Moreover, the Examiner has not established that Wang describes "determining whether [a] synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency," as claimed. For this claim limitation, the Examiner referred to paragraph [0053], which states that "[i]f the PLL detection circuit 17 is locked, the first phase detector 6 is switched on." Checking the status of a PLL detection circuit, however, does not constitute "determining whether [a] synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency," as claimed. Since Wang does not teach or suggest each and every element of claim 14, Applicants respectfully request that the rejection under 35 U.S.C. § 102(e) be withdrawn."

   The examiner respectfully disagrees. The limitation under discussion is as cited "determining whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency."

   Wang et al discloses in the abstract "intermediate frequency phase-locked loop detector (17) for supplying an output signal indicating whether an intermediate

frequency demodulator is in an unlocked mode which is the case if the incoming signal frequency does not correspond to a valid channel frequency." This indicates the phase locked loop will output a signal indicating the locked or unlocked status. The status of the phase locked loop must be determined in order to output a signal indicating an unlocked or locked signal. Paragraphs 0016 discloses "closing the synchronization phase control loop only if the PIF phase locked loop is locked (or more general, if the PIF demodulator does not comprise a phase locked loop, when a detector coupled to the PIF demodulator detects a locked state indicating that it is very likely that a valid channel frequency is detected." Paragraph 35 discloses "if the PLL is in lock and a video property is detected, the logic outputs of the detection circuits 17 and 18 will both be "1" and as a result "1" is supplied to the first phase detector control circuit 19 to close the phase control loop 6,8,10 and enable the first phase detector to pass the horizontal synchronization signal H.sync for synchronization of the OSD display with the incoming signal." Paragraph 36 discloses "if the PLL detection circuit 17 does not indicate a "Lock" or if there is no video property in the incoming signal, a logic "0" is supplied to the first phase detector control circuit 19 to open the phase control loop 6,8,10 ..." Paragraphs 35 and 36 discloses determining the status of the phase locked loop and determining whether the phase locked loop is still hunting or whether it is locked.

b. The applicant further contends

"Independent claim 1 recites, among other things, "[a] phase locked loop [that] keeps [a] synchronization signal asserted as long as the phase locked loop is locked onto a data signal; and a timing circuit that measures a period of time that the synchronization signal is asserted and produces a lock signal if the synchronization signal is asserted for at least a specified period of time."
The Examiner asserted that Wang discloses a phase locked loop that "keeps [a] synchronization signal asserted as long as the phase locked loop is locked onto a data signal ([0053]); [and] produces a lock signal if the synchronization signal is asserted for a least a specified period of time ([0051-[0053]) ...." See Office Action, p. 3. Applicants respectfully disagree. As a preliminary matter, it is unclear what portion of the cited passages corresponds to the claimed "synchronization signal" and clarification is respectfully requested. Moreover, contrary to the Examiner's assertion, Wang does not describe producing a lock signal if another signal is asserted for at least the pause time, Tp. Instead, Wang describes pausing a channel search during the time Tp to allow a coincidence detection circuit to reach a final value. See paragraphs [0043] and [0055].
Therefore, Wang does not teach or suggest each and every element of claim 1. Furthermore, van Roon, Transistors Tutorial, Lee, and IBM TDB, each relied on for their alleged teaching of various other claim limitations, fail to cure the deficiencies of Wang. Accordingly, Applicants respectfully submit that the Examiner has failed to set forth a prima facie case for obviousness and respectfully request that the rejection of claim 1, and corresponding dependent claims 2-8, be withdrawn."

The examiner respectfully disagrees. The limitation under discussion is as cited "a phase locked loop asserts a synchronization signal in the hunting mode when a hunting frequency passes through a data signal frequency and wherein the phase locked loop keeps the synchronization signal asserted as long as the phase locked loop is locked onto a data signal."

Paragraph 35 discloses "if the PLL is in lock and a video property is detected, the logic outputs of the detection circuits 17 and 18 will both be "1" and as a result "1" is supplied to the first phase detector control circuit 19 to close the phase control loop 6,8,10 and enable the first phase detector to pass the horizontal synchronization signal H.sync for synchronization of the OSD display with the incoming signal." Paragraph 36 discloses "if the PLL detection circuit 17 does not indicate a "Lock" or if there is no video property in the incoming signal, a logic

"0" is supplied to the first phase detector control circuit 19 to open the phase control loop 6,8,10 ..." Paragraphs 35 and 36 discloses determining the status of the phase locked loop and determining whether the phase locked loop is still hunting or whether it is locked.

Another limitation under discussion is "a timing circuit that measures a period of time that the synchronization is asserted and produces a lock signal if the synchronization signal is asserted for at least a specified period of time." Fig. 1 shows the output from the phase detector is inputted into the detector circuit, label 7. Paragraph 43 discloses "While status PC equals "1" the channel search is paused during the time Tp as indicated with status "1" of status signal CSS. During this time the control circuit 19 closes the phase locked loop comprising the first phase detector 6, the horizontal oscillator 8, and horizontal timing 10. This allows the coincidence detection circuit 7 to detect whether synchronization of the horizontal oscillator 8 with the incoming RF signal has been achieved (indicated with status "1" of status signal Cs)." Paragraph 31 discloses "the scanning of channel frequencies is paused during a time period Tp (indicated with status "1" in the channel search status CSS diagram)." The two paragraphs indicates that the phase locked loop connected to the coincidence detection circuit 7 is paused so the locked/unlocked status of the PLL can be examined for a time period of Tp.

c. The applicant further contends

"Claim 9 recites, among other things, "a controller chip having a phase locked loop that ... is adapted to operate in a locked mode that asserts the synchronization signal so long as the phase locked loop is locked onto a data signal; and a translation circuit that converts the synchronization signal from the controller chip to a lock signal ...." In contrast, the Examiner has not established that Wang discloses the aforementioned limitations. For example, the Examiner has not pointed to any description in Wang that corresponds to the claimed translation circuit. Applicants respectfully submit that this is because Wang discloses no such translation circuit. Furthermore, van Roon, Lee, and IBM TDB, each relied on for their alleged teaching of various other claim limitations, fail to cure the deficiencies of Wang. Accordingly, Applicants respectfully submit that the Examiner has failed to set forth a prima facie case for obviousness and respectfully request that the rejection of claim 9, and corresponding dependent claims 10-13, be withdrawn."

The examiner respectfully disagrees. The limitation under discussion is "a controller chip having a phase locked loop that .... Is adapted to operate in a locked mode that asserts the synchronization signal so long as the phase locked loop is locked onto a data signal".

Paragraph 35 discloses "if the PLL is in lock and a video property is detected, the logic outputs of the detection circuits 17 and 18 will both be "1" and as a result "1" is supplied to the first phase detector control circuit 19 to close the phase control loop 6,8,10 and enable the first phase detector to pass the horizontal synchronization signal H.sync for synchronization of the OSD display with the incoming signal." Paragraph 36 discloses "if the PLL detection circuit 17 does not indicate a "Lock" or if there is no video property in the incoming signal, a logic "0" is supplied to the first phase detector control circuit 19 to open the phase control loop 6,8,10 ..." Paragraphs 35 and 36 discloses determining the status of the phase locked loop and determining whether the phase locked loop is still hunting or whether it is locked.

Another limitation under discussion is "a translation circuit that convert a synchronization signal form the controller chip to a lock signal ..." Fig. 1 shows the output from the phase detector is inputted into the detector circuit, label 7. Paragraph 43 discloses "While status PC equals "1" the channel search is paused during the time Tp as indicated with status "1" of status signal CSS. During this time the control circuit 19 closes the phase locked loop comprising the first phase detector 6, the horizontal oscillator 8, and horizontal timing 10. This allows the coincidence detection circuit 7 to detect whether synchronization of the horizontal oscillator 8 with the incoming RF signal has been achieved (indicated with status "1" of status signal Cs)." Paragraph 31 discloses "the scanning of channel frequencies is paused during a time period Tp (indicated with status "1" in the channel search status CSS diagram)." The two paragraphs indicate that the phase locked loop connected to the coincidence detection circuit 7 is paused so the locked/unlocked status of the PLL can be examined for a time period of Tp.

d. The applicant further contends

"Applicants respectfully submit that insofar as the rejections of claims 15-18 rely on the unsupported assertions regarding the disclosure of Wang advanced by the Examiner in connection with the rejection of claim 14, such rejection lacks an adequate foundation, for at least the reasons outlined at section I above. Furthermore, van Roon, Lee, and IBM TDB, each relied on for their alleged teaching of various other claim limitations, fail to cure the deficiencies of Wang. Accordingly, the rejections of claims 15-18 should be withdrawn. "

The examiner respectfully disagrees. Claims 15-18 depend on claim14. Please refer to the rebuttal stated above for claim 14.

e. The applicant further contends

"Claim 19 requires, among other things, "a comparator circuit that compares the output signal [from a timing circuit] with a reference signal." The Examiner proposed combining a comparator circuit in Lee with a timing circuit in van Roon. The symbol timing and field sync restorer 114 in Lee, which was identified as the claimed comparator circuit (see Office Action, p. 10), compares a field reference signal with a field sync (see Lee, col. 2, lines 51-55). However, the field sync is constituted of 832 symbols (see Lee, col. 3, lines 10 and 11), whereas the timing circuit of van Roon outputs only one bit of data (see van Roon, Figure 3, p. 2). Thus, in the proposed combination, restorer 114 of Lee would compare a field reference signal with the one bit output from the van Roon timing circuit instead of the 832 symbol field sync. The comparison would therefore not be feasible or would at best yield meaningless results and the device would be unsatisfactory for its intended purpose of equalizing using a reference signal. See Lee, Title. Furthermore, Transistors Tutorial and IBM TDB, each relied on for their alleged teaching of various other claim limitations, fail to cure the deficiencies of the proposed combination of Lee and van Roon. Accordingly, Applicants respectfully submit that the Examiner has failed to set forth a primafacie case for obviousness and respectfully request that the rejection of claim 19, and corresponding dependent claims 20-26, be withdrawn."

Regarding claim 19, Applicant's arguments with respect to the rejection(s) of claim(s) 19 under Lee in view of Van Roon have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Hirai (US Publication No.: 20020180540) in view of Van Roon (NPL). Please see the rejection below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claim 14** is rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al. (U.S. Pub. No. 2004/0179138).

   a. **Claim 14**, Wang discloses

   - receiving an asserted synchronization signal from a phase locked loop, the phase locked loop disposed on the controller chip (abstract, lines 5-6, 9-11, 12-15);
   - determining whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency (abstract, lines 5-6, 9-11, 12-15, [0053])
   - asserting a lock signal if the phase locked loop has locked onto a data signal ([0051]-[0053], the synchronization signal from the synchronization phase locked

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-3, 9, 10, and 15** rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 2004/0179138) in view of Van Roon (NPL).

   a. **Claims 1,9**, Wang discloses:

- a controller chip that includes a phase locked loop adapted to operate in a hunting mode and a locked mode (abstract, lines 2-4 describes search, or hunting, mode, abstract, lines 6-11 describe locked mode)
- the phase locked loop asserts a synchronization signal in the hunting mode when a hunting frequency passes through a data signal frequency (abstract, lines 5-6, 9-11, 12-15)
- the phase locked loop keeps the synchronization signal asserted as long as the phase locked loop is locked onto a data signal ([0053]);
- produces a lock signal if the synchronization signal is asserted for a least a specified period of time ([0051]-[0053], the synchronization signal from the synchronization phase locked loop is asserted if the valid channel frequency is held for a predetermined time, Tp).
- Wang fails to disclose and a timing circuit that measures a period of time, Tp, that the synchronization signal is asserted, however, Van Roon discloses a simple timer for timing a signal (p. 2, fig. 3). Because the 555 timer as disclosed by Van Roon offers the advantages of being an inexpensive, stable, and user friendly integrated circuit (p. 1, line 2), it would have been obvious to one skilled in the art at the time of invention to use the timer as disclosed by Van Roon in the invention of Wang.

b. **Claim 2**, Wang fails to disclose a timing circuit which is an analog timer comprising a capacitor and a resistor network. However, an analeg timer which includes a capacitor and a resistor network is extremely well known in the art.

Van Roon discloses a analog timer with a capacitor and resistor network (p. 2, fig. 3). Because the 555 timer as disclosed by Van Roon offers the advantages of being an inexpensive, stable, and user friendly integrated circuit (p. 1, line 2), it would have been obvious to one skilled in the art at the time of invention to use the timer as disclosed by Van Roon in the invention of Wang.

c. **Claim 3**, although Wang fails to disclose the timing circuit comprises a transistor for resetting the timing circuit, Van Roon discloses a transistor for resetting the circuit (p. 3, 4-2, pin 4 is reset by transistor Q25). Because the 555 timer as disclosed by Van Roon offers the advantages of being an inexpensive, stable, and user friendly integrated circuit (p. 1, line 2), it would have been obvious to one skilled in the art at the time of invention to use the timer as disclosed by Van Roon in the invention of Wang.

d. **Claim 10**, Wang further discloses the translation circuit comprising a timer that measures a period of time that the synchronization signal is asserted ([0051]-[0053], the synchronization signal from the synchronization phase locked loop is asserted if the valid channel frequency is held for a predetermined time, Tp).

e. **Claim 15**, Wang further discloses determining that the synchronization signal is caused by the phase locked loop locking onto the data signal if the period of time that the synchronization signal is asserted is greater than a specified period of time ([0051]- [0053], the synchronization signal from the synchronization phase locked loop is asserted if the valid channel frequency is held for a predetermined time, Tp);

Wang fails to disclose measuring a period of time that the synchronization signal is asserted, Tp, however, Van Roon discloses a simple timer for timing a signal (p. 2, fig. 3). Because the 555 timer as disclosed by Van Roon offers the advantages of being an inexpensive, Stable, and user friendly integrated circuit (p. 1, line 2), it would have been obvious to one skilled in the art at the time of invention to use the timer as disclosed by Van Roon in the invention of Wang.

5. **Claims 4 and 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 2004/0179138) and Van Roon as applied to claim 3"above, and further in view of Transistors Non-Patent Literature.

   a. **Claim 4**, Van Roon fails to disclose the type of transistors used in his timer, however, Transistors Non-Patent Literature discloses transistor is at least one of a PNP and NPN bipolar junction transistor (p. 3, The NPN Transistor). Because NPN transistor are well known in the art as low cost transistor with low power consumption at low voltage levels, it would have been obvious to one skilled in the art at the time of invention to incorporate a NPN transistor as disclosed by Transistors Non-Patent Literature into the combined invention disclosed by Van Roon and Wang.

   b. **Claim 5**, Van Roon fails to disclose the type of transistors used in his timer, however, Transistors Non-Patent Literature discloses transistor is a field effect transistor (p. 3, FET's as Transistors). Because FET transistor are well known in the art as low cost transistor which canoperate at high voltage levels, it would

have been obvious to one skilled in the art at the time of invention to incorporate a FET transistor as disclosed by Transistors Non-Patent Literature into the combined invention disclosed by Van Roon and Wang.

6. **Claims 16 and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 2004/0179138) as applied to claim 14 above, and further in view of Lee (U.S. Patent No. 5,886,748).

   a. **Claim 16**, although Wang fails to disclose an input level detector that compares the synchronization signal with a reference signal and produces logical signals that may be fed into the timing circuit, Lee discloses comparing the synchronization signal with a reference signal and producing logical signals that may be fed into the timing circuit (col. 2, lines 51-55). Because this signal allows for more effective and accurate synchronization of the signal, it would be obvious to one skilled in the art at the time of invention to incorporate the comparator as disclosed by Lee into the invention of Wang.

   b. **Claim 17**, although Wang fails to disclose comparing the lock signal with a reference signal to produce the lock signal, Lee discloses comparing the lock signal with a reference signal to produce the lock signal (col. 2, lines 51-55). Because this signal allows for more effective and accurate synchronization of the signal, it would be obvious to one skilled in the art at the time of invention to incorporate the comparator as disclosed by Lee into the invention of Wang.

7. **Claim 6, 7, 11, and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 2004/0179138) and Van Roon (NPL) as applied to claim 2 above, and further in view of Lee (U.S. Patent No. 5,886,748).

   a. **Claims 6, 11, 12**, neither Wang nor Van Roon disclose an input level detector that compares the synchronization signal with a reference signal and produces logical signals that may be fed into the timing circuit, Lee discloses comparing the synchronization signal with a reference signal and producing logical signals that may be fed into the timing circuit (col. 2, lines 51-55). Because this signal allows for more effective and accurate synchronization of the signal, it would be obvious to one skilled in the art at the time of invention to incorporate the comparator as disclosed by Lee into the invention of Wang.

   b. **Claim 7**, neither Wang nor Van Roon disclose a comparator that receives a signal from the capacitor and resistor network and a reference signal as input and that outputs the lock signal to the host device based on the value of the reference signal compared to the signal from the capacitor and resistor network, Lee discloses comparing the a timing signal such as that which comes from the capacitive resistive network as disclosed by Van Roon with a reference signal and producing logical timing signals (col. 2, lines 51-55). Because this signal allows for more effective and accurate synchronization of the signal, it would be obvious to one skilled in the art at the time of invention to incorporate the comparator as disclosed by Lee into the invention of Wang.

8. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 2004/0179138), Van Roon (NPL), and Lee (U.S. Patent No. 5,886,748) as applied to claim 7 above, and further in view of IBM Technical Disclosure Bulletin, May 1990.

   a. **Claim 8**, neither Wang, nor Van Roon, nor Lee disclose a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value. However, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator includes feedback that changes alogical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value (see part 3 and figure 2). Thedisclosure further states that this scheme has the advantage of providing a stabilized synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the art a the time of invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the combined invention of Wang, Van Roon and Lee.

9. **Claim 13** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (u.s. Pub. No. 2004/0179138), Van Roon (NPL), and Lee (U.S. Patent No. 5,886,748) as applied to claim 12 above, and further in view of IBM Technical Disclosure Bulletin, May 1990.

a. **Claim 13**, neither Wang nor Lee disclose a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value. However, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value (see part 3 and figure 2). The disclosure further states that this scheme has the advantage of providing a stabilized synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the art a the time of invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the combined invention of Wang and Lee.

10. **Claim 18** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 2004/0179138) as applied to claim 14 above, and further in view of IBM Technical Disclosure Bulletin, May 1990.

a. **Claim 18**, Wang fails to disclose a comparator includes feedback that ch.anges a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value. However, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater

than a hysteresis threshold value (see part 3 and figure 2). The disclosure further states that this scheme has the advantage of providing a stabilized synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the art a the time of invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the invention of Wang.

11. **Claims 19,20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai (US Patent No.: 6794944) in view of Van Roon (NPL).

a. **Claim 19**, Hirai discloses

- "a comparator circuit that compares the output signal with a reference signal such that a lock signal is asserted based on the comparison of the output signal with the reference signal. (Fig. 1, label 23, Abstract discloses "a comparison circuit 23 for inputting and comparing count values of the counters 21 and 22 and outputting a control signal in an active state when the count value of the counter 21 is a first value and the count value of the counter 22 is the first value.")

Hirai fails to disclose

- a timing circuit that measures a period of time that a signal is asserted
- the timing circuit uses a capacitor
- wherein the timing circuit generates an output signal having a voltage across the capacitor.

However, Van Roon discloses

- a timing circuit that measures a period of time that a signal is asserted (fig. 2, 3)
- the timing circuit uses a capacitor (p. 2, fig. 3)
- wherein the timing circuit generates an output signal having a voltage across the capacitor (see pin 3 output of fig. 4-2)

Because the 555 timer as disclosed by Van Roon offers the advantages of being an inexpensive, stable, and user friendly integrated circuit (p. 1, line 2), it would have been obvious to one skilled in the art at the time of invention to use the timer as disclosed by Van Roon in the invention of Hirai.

b. **Claim 20**, although Hirai fails to disclose the timing circuit comprises a transistor for resetting the timing circuit, Van Roon discloses a transistor for resetting the circuit (p. 3, 4-2, pin 4 is reset by transistor Q25). Because the 555 timer as disclosed by Van Roon offers the advantages of being an inexpensive, stable, and user friendly integrated circuit (p. 1, line 2), it would have been obvious to one skilled in the art at the time of invention to use the timer as disclosed by Van Roon in the invention of Hirai.

12. **Claim 21** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai in view of Van Roon (NPL) as applied to claim 20 above, and further in view of Transistors Non-Patent Literature.

a. **Claim 21**, Van Roon fails to disclose the type of transistors used in his timer, however, Transistors Non-Patent Literature discloses transistor is at least one of a PNP and NPN bipolar junction transistor (p. 3, The NPN Transistor). Because NPN transistor are well known in the art as low cost transistor with low power consumption at low voltage levels. It would have been obvious to one skilled in the art at the time of invention to incorporate a NPN transistor as disclosed by Transistors Non-Patent Literature into the combined invention disclosed by Van Roon and Hirai.

13. **Claims 22-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai in view of Van Roon (NPL) as applied to claim 19 above, and further in view of IBM Technical Disclosure Bulletin, May 1990.

a. **Claims 22, 23**, neither Hirai nor Van Roon, nor Lee disclose a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value. However, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value (see part 3 and figure 2). The disclosure further states that this scheme has the advantage of providing a stabilized synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the

art a the time of invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the combined invention of Van Roon and Hirai.

b. **Claim 24**, Hirai discloses comparing the synchronization signal with a reference signal and producing logical signals that may be fed into the timing circuit (Fig. 1, label 23, Abstract discloses "a comparison circuit 23 for inputting and comparing count values of the counters 21 and 22 and outputting a control signal in an active state when the count value of the counter 21 is a first value and the count value of the counter 22 is the first value.").

c. **Claim 25**, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator circuit asserts a lock signal when the voltage across the capacitor exceeds the reference signal (see part 3 and figure 2). The combined invention of Lee, Van Roon, and the IBM Technical Disclosure Bulletin, May 1990 does not disclose expressly the capacitor charges slowly and discharges quickly. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use a capacitor which charges slowly and discharges quickly. Applicant has not disclosed that the capacitor charges slowly and discharges quickly provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with Hirai, Van Roon, and the IBM Technical Disclosure Bulletin, May 1990. Therefore, it would have been obvious to one of ordinary skill in this art to modify Hirai, Van Roon,

and the IBM Technical Disclosure Bulletin, May 1990 to obtain the invention as specified in claim 25.

d. **Claim 26**, IBM Technical Disclosure Bulletin, May 1990 discloses comparator asserts a lock signal when the reference signal exceeds the voltage across the capacitor see part 3 and figure 2). The combined invention of Lee, Van Roon, and the IBM Technical.

Disclosure Bulletin, May 1990 does not disclose expressly the capacitor charges slowly and discharges quickly. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use a capacitor which charges quickly and discharges slowly. Applicant has not disclosed that the capacitor charges quickly and discharges slowly provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with Hirai, Van Roon, and the IBM Technical Disclosure Bulletin, May 1990. Therefore, it would have been obvious to one of ordinary skill in this art to modify Hirai, Van Roon, and the IBM Technical Disclosure Bulletin, May 1990 to obtain the invention as specified in claim 25.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Meltzer (US Publication No.: 20030112915)

b. Lee (US Publication No.: 20020094054)

c. Eom (US Publication No.: 20020084859)

d. Nishimura et al (US Patent No.: 6392641).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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9/28/2007

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